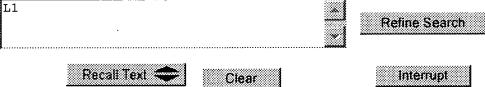
Search Results -

Terms	Documents
(bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)	4

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Set Name Query side by side

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DB=PGPB, USPT, USOC; PLUR=YES; OP=OR

<u>L1</u> (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3) 4 <u>L1</u>

Interrupt

Refine Search

Search Results -

Terms	Documents
(bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3)	0

US Pre-Grant Publication Full-Text Database US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database Database: JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins L2

Recall Text 4

Search:

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Search History

Clear

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Set Name Query **Hit Count Set Name** side by side result set DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3) L2 <u>L2</u> DB=PGPB,USPT,USOC; PLUR=YES; OP=OR L1 (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3) L1

### Search Results -

Terms	Documents
arbitration and (grant\$3 same concurrent same latenc\$3)	10

Database:

Database:

Database:

Database:

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Database:

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L3

Recall Text

Clear

Interrupt

# Search History

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Hit Count S	Set Name result set
10	<u>L3</u>
0	<u>L2</u>
4	<u>L1</u>
	10

### Search Results -

Terms	Documents
arbitration and (grant\$3 same concurrent same latenc\$3)	0

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L4

Refine Search
Recall Text
Clear
Interrupt

# **Search History**

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DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L4</u> arbitration and (grant\$3 same concurrent same latenc\$3)	0	<u>L4</u>
DB=PGPB, USPT, USOC; PLUR=YES; OP=OR		
<u>L3</u> arbitration and (grant\$3 same concurrent same latenc\$3)	10	<u>L3</u>
DB=EPAB, $JPAB$ , $DWPI$ , $TDBD$ ; $PLUR=YES$ ; $OP=OR$		
<u>L2</u> (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3	) 0	<u>L2</u>
DB=PGPB, $USPT$ , $USOC$ ; $PLUR=YES$ ; $OP=OR$		
L1 (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3	) 4	<u>L1</u>

Interrupt

# Refine Search

### Search Results -

Terms	Documents
(grant\$3 same concurrent same latenc\$3)	11

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US OCR Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
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L5

Refine Search

Recall Text 4

# Search History

Clear

# DATE: Friday, November 04, 2005 Printable Copy Create Case

Set Name Query	Hit Count	Set Name
side by side		result set
DB=PGPB, $USPT$ , $USOC$ ; $PLUR=YES$ ; $OP=OR$		
<u>L5</u> (grant\$3 same concurrent same latenc\$3)	11	<u>L5</u>
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L4</u> arbitration and (grant\$3 same concurrent same latenc\$3)	0	<u>L4</u>
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L3</u> arbitration and (grant\$3 same concurrent same latenc\$3)	10	<u>L3</u>
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L2</u> (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3	) 0	<u>L2</u>
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L1</u> (bus near3 arbitration) and (grant\$3 same concurrent same latenc\$3	) 4	<u>L1</u>



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# SAMBA-bus: A high performance bus architecture for system-on-chips

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and up to 15 times reduction in the average communication latency. In addition, the performance of SAMBA-bus architecture is affected only compared with a traditional bus architecture, the SAMBA-bus architecture can have up to 3.5 times improvement in the effective bandwidth, slightly by arbitration latency, because bus transactions can be performed without waiting for the bus access grant from the arbiter. This feature is desirable in SoC designs with large numbers of modules and long communication delay between modules and the **bus** arbiter. transactions can be performed simultaneously with only a single **bus** access **grant** from the **bus** arbiter. Experimental results show that, A high performance communication architecture, SAMBA-bus, is proposed in this paper. In SAMBA-bus, multiple compatible bus

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asynchronous circuits, circuit CAD, system buses, system-on-chip

Non-controlled Indexing

SAMBA bus architecture. SOC design arbitration latency, bus arbiter high performance bus architecture, high performance communication architecture, long communication delay, multiple compatible bus transactions, system-on-

chip traditional bus architecture

Author Keywords Not Available

References

No references available on IEEE Xplore.

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